XI. SIM4-01/SIM4-02 PROTOTYPING SYSTEM

A. General System Description

During the development phase of the equipment using the MCS-4 microcomputer set, the designer will often find it helpful to have a means for testing out his program. An interface circuit in which 1701 or 1702 electrically programmable and erasable read only memories simulate the 4001 mask programmable read only memories will help serve this purpose. Using this interface, it is possible for the system designer to program the 1701's or 1702's, plug them into the system, check out the programs and make corrections as necessary. In this way, the development check-out cycle can be typically reduced to one hour or less. With mask programmable ROM's, this cycle is usually four to six weeks. Intel has developed two microcomputer prototyping kits, SIM4-01 and SIM4-02, which use the electrically programmable and erasable ROM.

The maximum directly addressable system configuration is available with the SIM4-02. The 4004 CPU directly controls up to sixteen 1701's or 1702's and up to sixteen RAMs. Eight ROM output ports and eight ROM input ports are provided. These ports are associated with the first eight ROM in the system. Of course, the user must be aware that individual lines of a ROM port can be used for input or output but not both. The input-output option is of course fixed at the time that the 4001 is mask-programmed. Sixteen RAM output ports are also provided. In addition, all data, timing, and memory controls signals are brought to the connector to permit future memory expansion.

The SIM4-01 is designed for small systems. This board contains provision for up to four 1701's or 1702's and four 4002's. It provides up to four RAM output ports (each port contains 4-bits), four ROM output ports and four ROM input ports.

Both systems come complete with the 4004 CPU and four 4002 RAMs. Additional RAMs and ROMs may be added as required. Sockets are provided on the boards for all MCS-4 components and for all ROMs. Note that all programs written for the SIM4-01 may be used without alterations on the SIM4-02.

IMPORTANT

It should be noted that the 1701 and 1702's are described in the data sheet with respect to "positive logic" (high level = p-logic 1). On the other hand the MCS-4 system is defined in terms of "negative logic" (low level = n-logic 1). As a result, when 1701 or 1702 ROM's are being programmed to simulate the 4001, characters should be defined as P = high level = n-logic 0 or an N = low level = n-logic 1. For instance, consider the instruction code for ADM (one of the 45 instructions for the MCS-4).

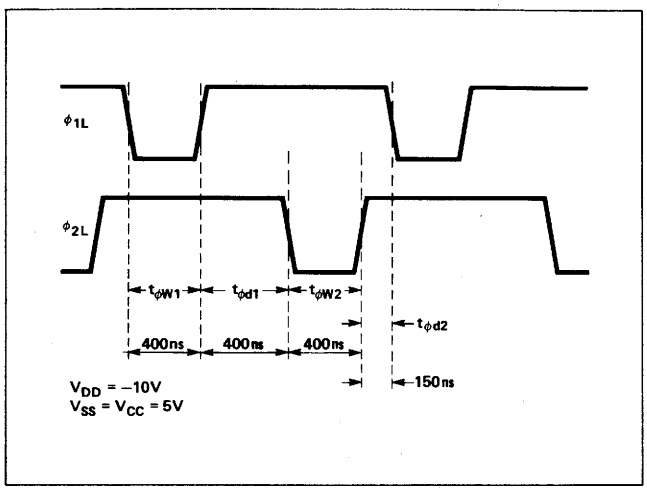
11101011

When preparing the program tape it should be typed,

BNNNPNPNNF

This is the code that will be put into the 4001 when the final system is defined. It will correctly simulate the 4001 operation when the 1701 or 1702 is used with the SIM4-01 or SIM4-02 system.

The schematics and block diagrams for both prototyping systems are shown on the following pages. The 4004 and the 4002's are used as they would be in a conventional system. Additional circuitry is used to simulate the 4001 ROM's. The two phase clocks are generated by the 9602 single shot multivibrator using discrete clock drivers.



Prototype System Clock Drivers

The 9316 counter together with the 3205 - one of eight decoder - serve to decode the cycle timing for the system, thus simulating one of the functions implemented on the 4001 chips. The output of the 3205 decoder indicates which cycle the unit is executing; i.e., the A_1, the A_2, the A_3, the M_1, etc. The discrete transistors serve to convert data bus levels to TTL levels and vice versa. Two 3404 hex latches are wired as the equivalent of three quad latch units. These latches act as address registers for the 1701 or 1702 memory array. The quad latch units are loaded on the A_1, A_2, and A_3 cycles respectively. Those address bits loaded during A_1 and A_2 drive the 1701 or 1702 address line directly, while a 3205 decoder is used to generate the chip select signals for the 1701 or 1702 memory array from the four bits loaded during A_3. Two such decoders would be used if a full array of sixteen 1701's or 1702's were to be utilized. The output of the 1701 or 1702 array is one byte or 8 bits wide. A multiplexer is used to gate four bits at a time onto the four bit wide data bus. The first four bits are selected on the M_1 cycle, the second four bits on the M_2 cycle. The signals at the output of the multiplexer are at TTL levels. These levels are converted to the MOS levels on the 4004 data bus by means of a set of four discrete level shifter circuits. The pull down resistors for these circuits are connected via diode disconnects to a pull down resistor activator circuit. This circuit is activated during the M_1 and M_2 cycles via the two input NAND gate driver. This driver receives two of its three inputs from the M_1 and M_2 decoder.

The balance of the circuitry shown in the schematic is used to implement the input/output port functions associated with the 4001 read only memories. The execution of an SRC instruction (which is used to activate a port) is indicated to the port control circuitry by the presence of the command signal at X_2 time. This condition is decoded and used to load a two latch port selection register. The contents of this register

are in turn decoded by means of four two-input NAND gates. Execution of a port control instruction is indicated by the presence of the command signal ($\overline{CM}$) during M_2 time combined with the appropriate code on the data bus. For instance the READ ROM INPUT condition is detected by a seven-input NAND gate. When this instruction is detected a flip-flop consisting of two-input NAND gates is set. (The presence of a "1" in the port read-control flip-flop is used to enable the inputs from one of two multiplexers onto the data bus during X_2 time.) Data is then transferred into the 4004 from an input port at X_2 time. The port read-control flip-flop is reset at X_3 time so that it will not influence operations on the instruction.

In general, the number of output ports provided by the array of 4002s is adequate. However, to fully duplicate the effects of the 4001s, it may be necessary to implement ROM output ports as well as input ports. Although the two latch port selection register and decoder need not be duplicated, another seven-input NAND gate together with a flip-flop is provided to detect the condition for a WRITE ROM OUTPUT port. A four bit latch is provided for each output port to be implemented. During the subsequent X_2 cycle, the data on the data bus is loaded into the selected port latches. These latches then retain the data. The flip-flop controlling this operation should also be reset at X_3 time. The ROM outputs invert the output data and are TTL compatible. RAM outputs are MOS compatible. Refer to the schematics and pin configurations for both the SIM4-01 and SIM4-02.

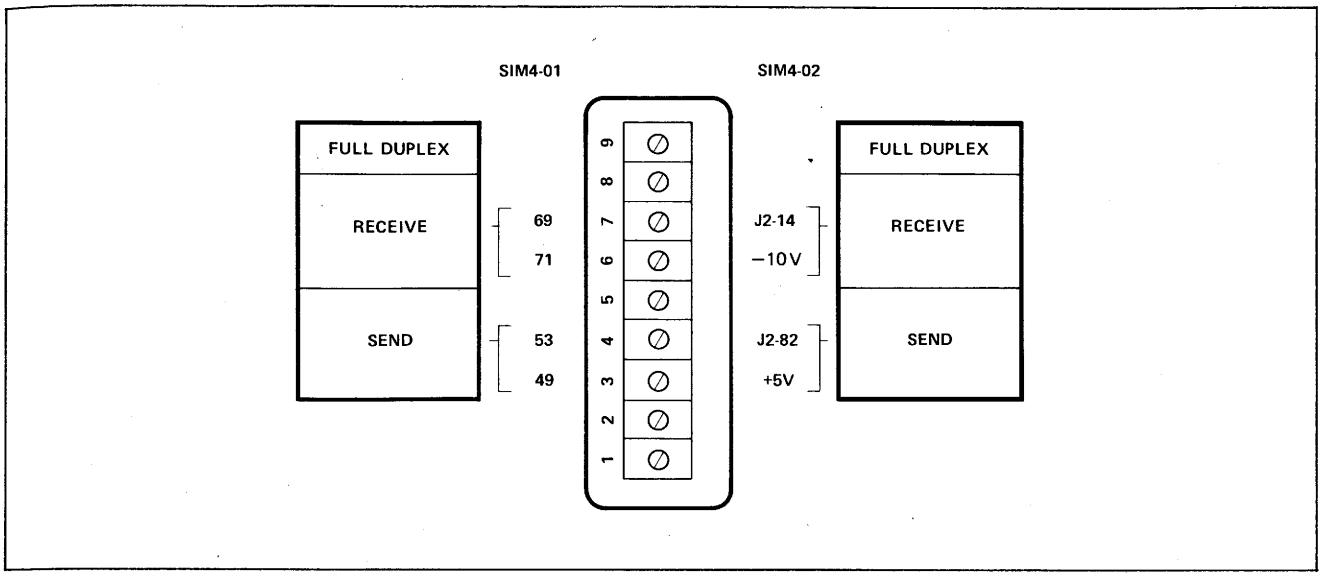
Discrete interface circuits are provided on the cards to communicate with a teletype. Data can be entered through the simulated ROM input ports either from the keyboard or the paper tape reader of the teletype. The receiving and transmitting of data are in serial form. Other terminal devices such as typical commercial keyboards, printers, LED's, CRTs and cassettes can readily communicate with the system with proper single interface.

These systems may be reset to zero by using a RESET switch as indicated on the board pin connector list. Debouncing for the switch is provided on the board.

The TEST signal may be transmitted directly to the TEST pin of the 4004 or through a debouncer and one-shot multivibrator. When the TEST signal comes from the one-shot, the program executed by the CPU should be looping through a JCN instruction waiting for TEST signal.

Teletype Interface

The MCS-4 is designed to operate with all types of terminal devices. A typical example of peripheral interface is the teletype (ASR-33). The SIM4 contains three simple transistor TTY interface circuits. Refer



Teletype Terminal Strip
(See Appendix D for details)

to the appropriate SIM4 schematics for the actual circuit diagrams. One transistor is used for receiving serial data from the teletype, one for transmitting data back to the teletype, and the third for tape reader control.

The teletype must be operating in the full duplex mode. Refer to your teletype operating manual for making connections within the TTY itself. Since all teletypes are not identical, it is impossible to present a general interconnection scheme with either of the SIM4 boards. Many models include a nine terminal barrier strip in the rear of the machine. It is at this point where the connections are made for full duplex operation. The interconnections to the SIM4 for transmit and receive are made at this same point.

To use the teletype reader with the SIM4, the machine must contain a reader power pack. The contacts of a 10V dc relay must be connected in series with the TTY automatic reader (refer to TTY manual) and the coil is connected to the SIM4 tape reader control as shown. This relay must be supplied by the user.

Note that the SIM4 clock generator must remain set at 750 kHz.

In order to sense the start character, data in is also sensed at the TEST input. It requires approximately 110ms for the teletype to transmit or receive eight serial data bits plus three control bits. The first and last bits are idling bits, the second is the start bit, and the following eight bits are data. Each bit stays 9.09ms. While waiting for data to be transmitted, the 4004 is executing a JCN based on the TEST input. When the start character is received, the processor jumps to the TTY processing routine. Under software control, the processor can determine the duration of each bit and strobe the character at the proper time.

A listing of a teletype control program is shown in Section X, Part D.

CAUTION:

In one mode of operation, these prototype systems do not truly simulate the activity of the 4001. After the system is reset and the program counter in the CPU is returned to address zero, a two word instruction in the first two steps of the program may be improperly executed. (This is characteristic of the prototype boards, not of the MCS-4 components.) This is the result of an asynchronous reset pulse applied to the "simulated" 4001 ROM memory.

To insure proper operation of the prototype systems one of the following techniques must be implemented:

1. *Use a NOP in the first location of program memory (ADDRESS 0). Any other single word instruction may also be used.*
2. *Use the SYNC pulse to synchronize the reset signal to the system. Then the prototype system will truly simulate the program memory in the 4001.*

B. SIM4-01 / SIM4-02 Specifications

FEATURES:

• Complete Micro Computer System for Prototyping and/or Production • Reprogrammable ROMs Simulate 4001s • TTY Interface on Clock • Two Phase Clock Generator on Card • Test and Reset Signal Generator on Card

SIM4-01 SPECIFICATIONS

Card Dimensions:
8.4 inches high
5.7 inches deep

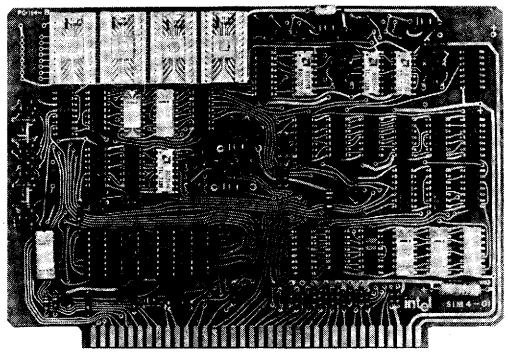
MCS-4 Components included on Board:
(sockets included for memory expansion)
one 4004
four 4002s

Maximum Memory Configuration:
four 4002 RAMs – 320 x 4
four 1702 ROMs – 1024 x 8

Operating Speed:
1.35 μs clock period
10.8 μs instruction cycle

DC Power Requirement:
Voltage–
$V_{CC} = V_{SS} = 5V \pm 5\%$
TTL GND = 0V
$V_{DD} = -10V \pm 5\%$
Current–
No load operation
I_{CC} = 1.5 amp
I_{DD} = 0.6 amp
Worst case loading (16 TTL inputs and outputs)
I_{CC} = 1.6 amp
I_{DD} = 1.5 amp

Connector:
a. Solder lug type/Amphenol
72 pin connector
P/N 225-23621-101
b. Wire Wrap type/Amphenol
72 pin connector
P/N 261-15636-2
c. Wire Wrap type/CDC
72 pin connector
P/N VPBOIE36300A1



SIM4-01 Prototyping Board

SIM4-02 SPECIFICATIONS

Card Dimensions:
11.5 inches high
9.5 inches deep

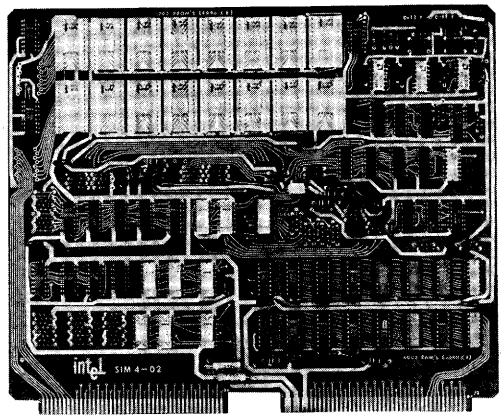
MCS-4 Components included on Board:
(sockets included for memory expansion)
one 4004
four 4002s

Maximum Memory Configuration:
sixteen 4002 RAMs – 1280 x 4
sixteen 1702 ROMs – 4096 x 8

Operating Speed:
1.35 μs clock period
10.8 μs instruction cycle

DC Power Requirement:
Voltage–
$V_{CC} = V_{SS} = 5V \pm 5\%$
TTL GND = 0V
$V_{DD} = -10V \pm 5\%$
Current–
No load operation
I_{CC} = 1.8 amp
I_{DD} = 0.95 amp
Worst case loading (32 TTL inputs and outputs)
I_{CC} = 2.75 amps
I_{DD} = 1.85 amp

Connector
Wire Wrap type/Amphenol
86 pin connector
P/N 261-10043-2



SIM4-02 Prototyping Board